Hochschule
München (HM)
University of
Applied Sciences

Laboratory for
Mechatronic
and Renewable
Energy Systems
(LMRES)

Optimal reference voltage saturation for nonlinear current control of synchronous machine drives

Niklas Monzen and Christoph M. Hackl
christoph.hackl@hm.edu

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Outline

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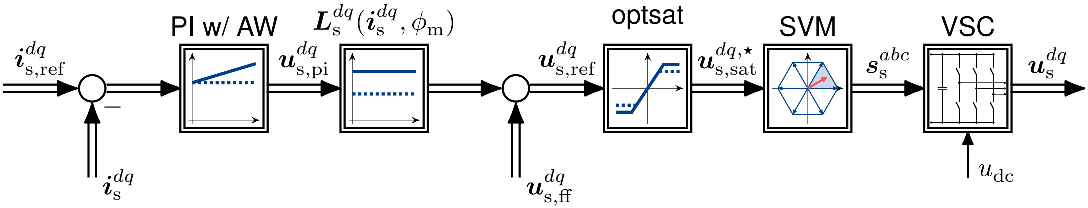
Introduction

Problem statement: Drawbacks of converters



Any voltage source converter (VSC) suffers from *four* inevitable drawbacks (D_i):

(D_1) voltage deterioration due to nonlinear current-dependent voltage drops over the semiconductors [1],

(D_2) voltage ripples due to the switching behavior of the power electronic devices [2],

(D_3) delayed voltage response due to modulation [3], and

(D_4) output voltage constraints due to a limited dc-link voltage.

$\Longrightarrow$ Here we will discuss and solve the last problem in an optimal way ("optsat")!

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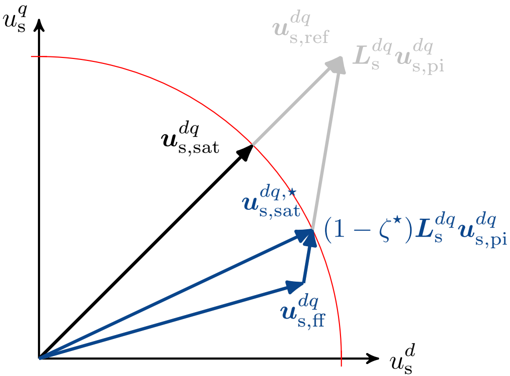
1 Introduction
- Problem statement
- Proposed solution

Introduction

Proposed solution: Illustration of the idea of **Optimal Reference Voltage Saturation (ORVS)**



☞ Consideration of **voltage hexagon** as constraint is possible! (another paper in preparation)

$$\widehat{u}_{s,max}(u_{dc}) := \begin{cases} \frac{u_{dc}}{2}, & \text{for PWM,} \\ \frac{u_{dc}}{\sqrt{3}}, & \text{for SVM.} \end{cases}$$

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2 Modeling and control

- Synchronous machine
- I/O linearization
- PI controller design with anti-windup
- Reference voltage saturation

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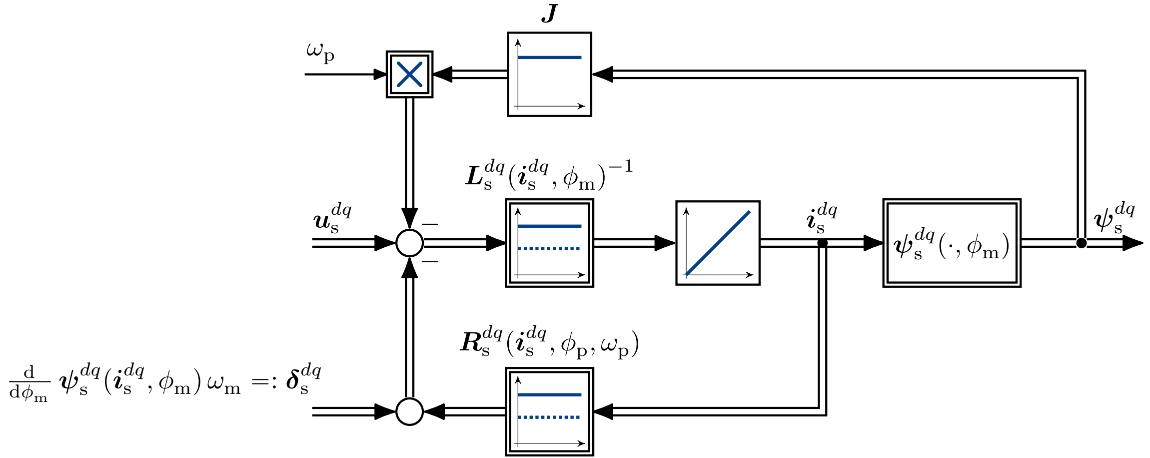
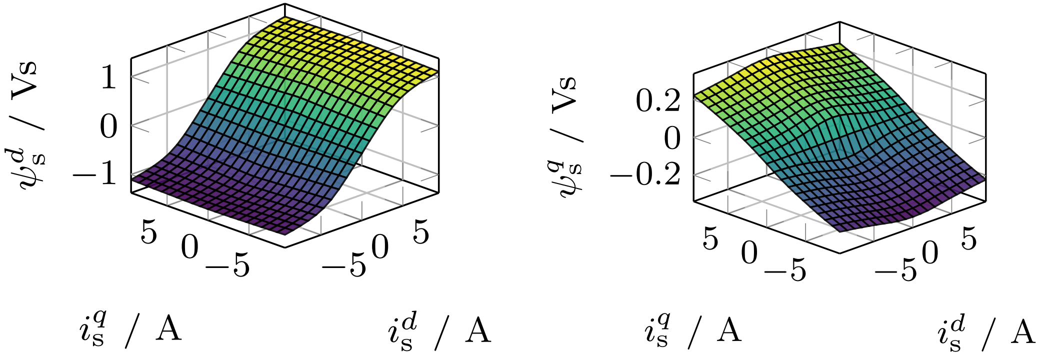
Modeling and control

Synchronous machine: Block diagram of nonlinear current dynamics with current- and angle-dependent differential inductances and flux linkages



Modeling and control

Synchronous machine: Nonlinear flux linkage maps ($\phi_\mathrm{m} = 0^\circ$)



(**a**) d-axis flux linkage map.

(**b**) q-axis flux linkage map.

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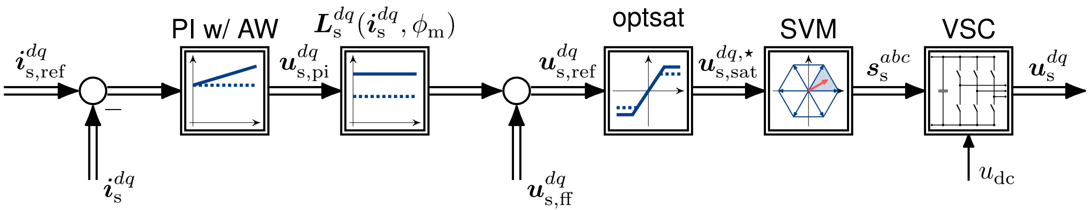
Modeling and control

Input/ouput (I/O) linearization



I/O linearization approach

$$\boldsymbol{u}_s^{dq} \approx \boldsymbol{u}_{s,ref}^{dq} := \boldsymbol{L}_s^{dq}\boldsymbol{u}_{s,pi}^{dq} + \underbrace{\boldsymbol{R}_s^{dq}\boldsymbol{i}_s^{dq} + \omega_p \boldsymbol{J}\boldsymbol{\psi}_s^{dq} + \boldsymbol{\delta}_s^{dq}}_{=:\boldsymbol{u}_{ff}^{dq}}, \tag{1}$$

gives simple **integral current dynamics** $\frac{d}{dt}\boldsymbol{i}_s^{dq} = \boldsymbol{u}_{s,pi}^{dq}$ and allows for simple PLL-like **tuning by pole placement** (for details see paper).

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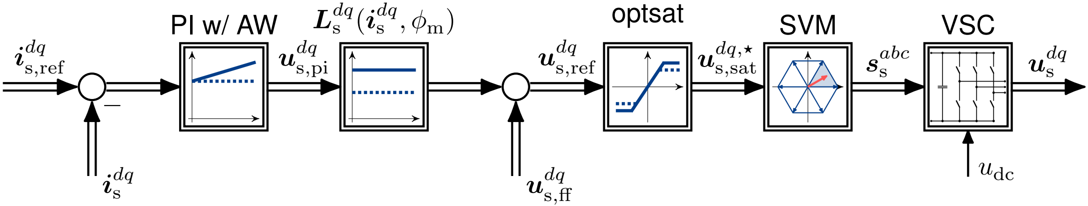

Current control system

$$\left.\begin{aligned} \boldsymbol{u}_{s,pi}^{dq} &= \boldsymbol{K}_p^{dq}\left(\boldsymbol{i}_{s,ref}^{dq} - \boldsymbol{i}_s^{dq}\right) + \boldsymbol{K}_i^{dq}\boldsymbol{x}_i^{dq}, \\ \frac{d}{dt}\boldsymbol{x}_i^{dq} &= f_{aw}\left(\widehat{u}_{s,max}, \boldsymbol{u}_{s,ref}^{dq}\right)\left(\boldsymbol{i}_{s,ref}^{dq} - \boldsymbol{i}_s^{dq}\right) \end{aligned}\right\} \tag{2}$$

with integral state $\boldsymbol{x}_i^{dq}$, gain matrices $\boldsymbol{K}_p^{dq}$ & $\boldsymbol{K}_i^{dq}$ and anti-windup (“conditional integration”) with

$$f_{aw}\left(\widehat{u}_{s,max}, \boldsymbol{u}_{s,ref}^{dq}\right) = \begin{cases} 0, & \text{if } \|\boldsymbol{u}_{s,ref}^{dq}\| > \widehat{u}_{s,max}, \\ 1, & \text{else.} \end{cases}$$

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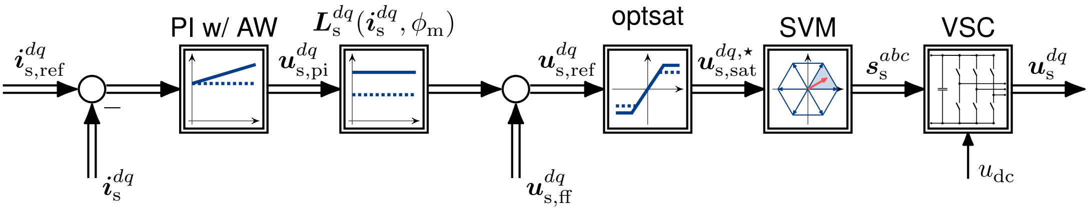
Modeling and control

Reference voltage saturation: Comparison of different approaches



- **optimal reference voltage saturation** [——] with

$$u^{dq,\star}_{s,sat} := \arg\min_{u^{dq}_s} \left\| \frac{d}{dt} i^{dq}_s(u^{dq}_{s,pi}) - \frac{d}{dt} i^{dq}_s(u^{dq}_s, \hat{u}_{s,max}) \right\| = \begin{cases} u^{dq}_{s,ref} \frac{\hat{u}_{s,max}}{\|u^{dq}_{s,ref}\|}, & \text{if } \|u^{dq}_{s,ff}\| \geqslant \hat{u}_{s,max}, \\ u^{dq}_{s,ff} + (1-\zeta^\star)\, L^{dq}_s u^{dq}_{s,pi}, & \text{if } \|u^{dq}_{s,ref}\| \geqslant \hat{u}_{s,max}, \\ u^{dq}_{s,ref}, & \text{else} \end{cases}$$

- **conventional saturation** [——] with $u^{dq}_{s,sat} := \begin{cases} u^{dq}_{s,ref} \frac{\hat{u}_{s,max}}{\|u^{dq}_{s,ref}\|}, & \text{if } \|u^{dq}_{s,ref}\| \geqslant \hat{u}_{s,max}, \\ u^{dq}_{s,ref}, & \text{else,} \end{cases}$

- **no saturation (and no anti-windup)** [——]

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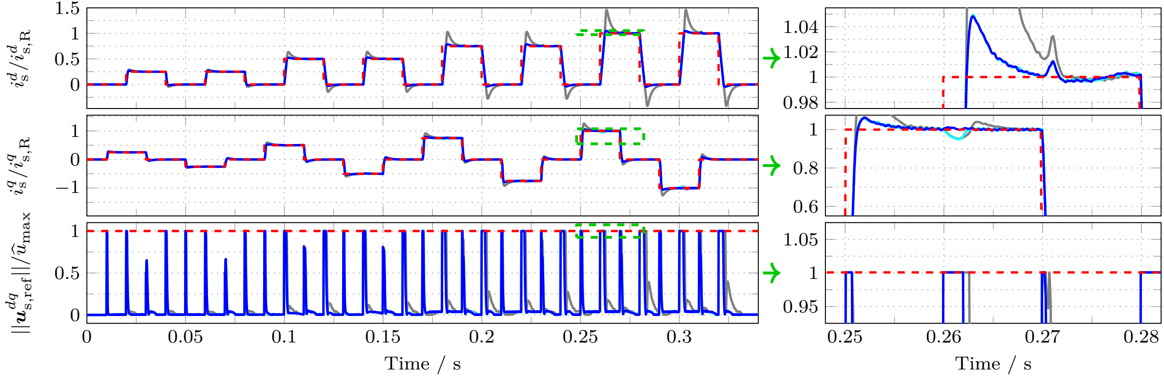
3 Validation

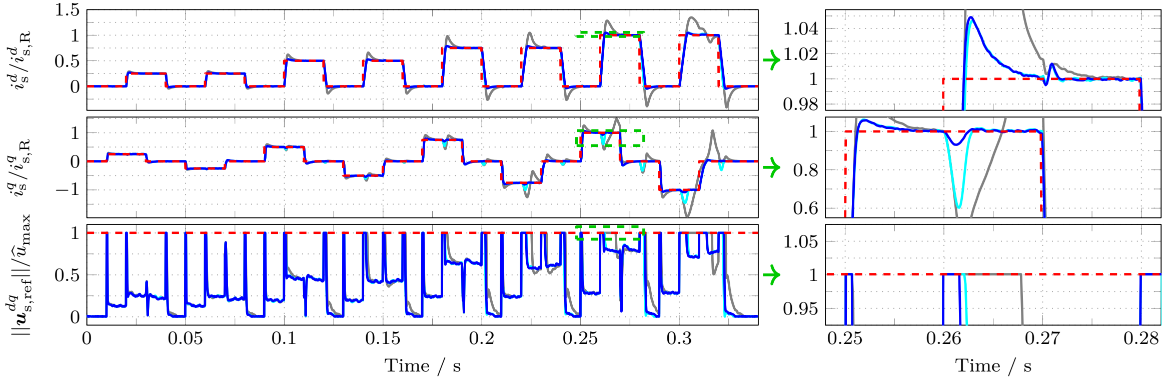
Validation

Simulation results at standstill ($\omega_m = 0$): Control system *with* ORVS [——], *with* conventional saturation [——] and *without* saturation and anti-windup [——]



Validation

Simulation results at rated speed ($\omega_{\mathrm{m}} = \omega_{\mathrm{m,R}}$): Control system *with* ORVS [blue line], *with* conventional saturation [cyan line] and *without* saturation and anti-windup [grey line]



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4 Conclusion

Conclusion

Summary and future work

To take home: **Optimal reference voltage saturation (ORVS)** allows to

- optimally exploit the available voltage
- optimally saturate the reference voltage by considering the limited dc-link voltage (voltage constraint)
- maintain the desired change of the current direction
- reduce overshoots
- mitigate undesired cross-coupling effects (at voltage limit)

Future work

- more extensive (experimental) validation
- consideration of voltage hexagon (already solved)
- application/extension to electrically-excited synchrouns machines or doubly-fed induction machines

References I

[1] Hag-Wone Kim, Myung-Joong Youn, Kwan-Yuhl Cho, and Hyun-Soo Kim. Nonlinearity estimation and compensation of PWM VSI for PMSM under resistance and flux linkage uncertainty. *IEEE Transactions on Control Systems Technology*, 14(4):589–601, 2006.

[2] Joachim Holtz and Xin Qi. Optimal control of medium-voltage drives—an overview. *IEEE Transactions on Industrial Electronics*, 60(12):5472–5481, 2013.

[3] V. Blasko, V. Kaura, and W. Niewiadomski. Sampling of discontinuous voltage and current signals in electrical drives: a system approach. 34(5):1123–1130.